







# ELECTRONIC INFORMATION DISCLOSURE STATEMENT

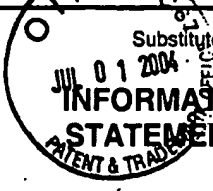
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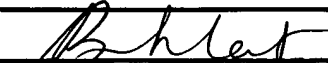
Title of Invention	Method and apparatus for performing technology mapping																												
<p>Application Number: 10/061719 </p> <p>Confirmation Number: 1570</p> <p>First Named Applicant: Steven Teig</p> <p>Attorney Docket Number: SPLX.P0098</p> <p>Art Unit: <del>2423</del> 2828</p> <p>Examiner: Kevin J. Teeke TAT</p> <p>Search string: ( 5668732 or 5696694 ).pn.</p> <p><b>US Patent Documents</b></p> <p>Note: Applicant is not required to submit a paper copy of cited US Patent Documents</p> <table border="1"><thead><tr><th>init</th><th>Cite.No.</th><th>Patent No.</th><th>Date</th><th>Patentee</th><th>Kind</th><th>Class</th><th>Subclass</th></tr></thead><tbody><tr><td>BT</td><td>1</td><td>5668732</td><td>1997-09-16</td><td>Khouja et al.</td><td></td><td></td><td></td></tr><tr><td>BT</td><td>2</td><td>5696694</td><td>1997-12-09</td><td>Khouja et al.</td><td></td><td></td><td></td></tr></tbody></table> <p><b>Signature</b></p> <table border="1"><thead><tr><th>Examiner Name</th><th>Date</th></tr></thead><tbody><tr><td></td><td>06/29/04</td></tr></tbody></table>		init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass	BT	1	5668732	1997-09-16	Khouja et al.				BT	2	5696694	1997-12-09	Khouja et al.				Examiner Name	Date		06/29/04
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 <p>Substitute for form 1449A/PTO</p> <p><b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b></p> <p>(use as many sheets as necessary)</p>				<b>Application Number</b>	10/061,719
				<b>Filing Date</b>	1/31/2002
				<b>First Named Inventor</b>	Steven Teig, et al.
				<b>Group Art Unit</b>	2125 2825
				<b>Examiner Name</b>	Kevin J. Teska TAT
<b>Sheet</b>	1	of	1	<b>Attorney Docket Number</b>	SPLX.P0098

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>6</sup>
BT	1.	Krishnamoorthy et al., Boolean Matching of Sequential Elements, Proceedings of the 31st annual conference on Design automation conference, pp. 691-697, June 06-10, 1994, San Diego, California, United States.	

<b>Examiner Signature</b>		<b>Date Considered</b>	09/29/04
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Substitute for form 1449A/PTO				Application Number	10/061,719
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				First Named Inventor	Steven Teig, et al.
				Group Art Unit	2125 2826
				Examiner Name	TRT
Sheet	2	of	2	Attorney Docket Number	SPLX.P0098

## OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

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BT	14.	D. Jongeneel, R. Otten, Y. Watanabe and R. K. Brayton, Area and Search Space Control for Technology Mapping, 37 <sup>th</sup> Design Automation Conference, 86-91, 2000.	
	15.	Henrik Reif Andersen, An Introduction to Binary Decision Diagrams, October 1997 (minor revisions April 1998), 36 pp.	
	16.	Jerry Burch and David Long, Efficient Boolean Function Matching, Proc. ICCAD 1992, 408-411.	
	17.	John Fishburn, A Depth-Decreasing Heuristic for Combinational Logic; or How to Convert Ripple-Carry Adder into a Carry-Lookahead Adder or Anything In-Between, Proceedings of the 27 <sup>th</sup> Design Automation Conference, 361-364, 1990.	
	18.	Kamal Chaudhary and Massoud Pedram, A Near Optimal Algorithm for Technology Mapping Minimizing Area under Delay Constraints, Proceedings of the 29 <sup>th</sup> Design Automation Conference, 492-498, 1992.	
	19.	Kurt Keutzer, DAGON: Technology Binding and Local Optimization by DAG Matching, Proceedings of the 24 <sup>th</sup> Design Automation Conference, 341-347, 1987	
	20.	Randal Bryant, Symbolic Boolean Manipulation with Ordered Binary Decision Diagrams, CMU CS Tech Report CMU-CS-92-160.	
	21.	Uwe Hinsberger and Reiner Kolla, Boolean Matching for Large Libraries, Proceedings of the 35 <sup>th</sup> Design Automation Conference, 206-211, June 1998.	
	22.	Yuji Kukimoto, Robert K. Brayton, and Prashant Sawkar, Delay-Optimal Technology Mapping by DAG Covering, Dept. of Electrical Engineering and Computer Science, University of California, Berkeley, Strategic CAD Laboratories, Intel Corp., October 1997.	
BT	23.	Zbigniew J. Czech, et al., An Optimal Algorithm for Generating Minimal Perfect Hashing Functions, Information Processing Letters, 43(5); 257-264, October 1992	

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Examiner Signature	<i>B. Hart</i>	Date Considered	01/29/04
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				First Named Inventor	Steven Teig, et al.
				Group Art Unit	2125 2826
				Examiner Name	Pat
Sheet	1	of	2	Attorney Docket Number	SPLX.P0098

RELATED U.S. PATENT APPLICATIONS					
Examiner Initials	Cite No. <sup>1</sup>	U.S. Patent Application Serial Number	Name of Patentee or Applicant of Cited Document	Date of Filing MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
Pat	1.	10/062,017	Steven Teig & Asmus Hetzel	01-31-02	
	2.	10/061,459	Steven Teig & Asmus Hetzel	01-31-02	
	3.	10/062,014	Steven Teig & Asmus Hetzel	01-31-02	
	4.	10/062,044	Steven Teig & Asmus Hetzel	01-31-02	
	5.	10/066,264	Steven Teig & Asmus Hetzel	01-31-02	
	6.	10/066,188	Steven Teig & Asmus Hetzel	01-31-02	
	7.	10/062,992	Steven Teig & Asmus Hetzel	01-31-02	
	8.	10/061,474	Steven Teig & Asmus Hetzel	01-31-02	
	9.	10/066,456	Steven Teig & Asmus Hetzel	01-31-02	
	10.	10/062,993	Steven Teig & Asmus Hetzel	01-31-02	
Pat	11.	10/062,047	Steven Teig & Asmus Hetzel	01-31-02	

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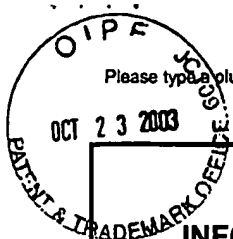
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Examiner* Initials	Cite No. <sup>1</sup>	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code <sup>2</sup> (if known)			
AS	12.	5,649,165		Jain et al.	07-15-97	
VA	13.	6,301,687	B1	Jain et al.	10-09-01	

Examiner Signature		Date Considered	09/28/04
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				<b>Filing Date</b>	1/31/02
				<b>First Named Inventor</b>	Steven Teig, et al.
				<b>Group Art Unit</b>	2123 <i>WJ</i>
				<b>Examiner Name</b>	<i>WJ</i>
<b>Sheet</b>	1	of	1	<b>Attorney Docket Number</b>	SPLX.P0098

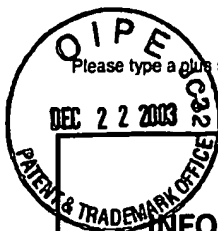
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Examiner* Initials	Cite No. <sup>1</sup>	U.S. Patent Document Number Kind Code <sup>2</sup> (if known)	Date of Publication MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
<i>BT</i>	1.	5,311,442	05-10-1994	Fukushima	<b>RECEIVED</b>  OCT 27 2003  Technology Center 2100	
	2.	5,526,276	06-11-1996	Cox et al		
	3.	5,752,000	05-12-1998	McGeer et al		
	4.	6,086,626	07-11-2000	Jain et al		
	5.	6,102,964	08-15-2000	Tse et al		
	6.	6,134,705	10-17-2000	Pedersen et al		
	7.	2001/013113	08-09-2001	Matsunaga		
	8.	6,298,472	10-02-2001	Phillips et al		
	9.	6,336,208	01-01-2002	Mohan et al		
	10.	6,473,884	10-29-2002	Ganai et al		
	11.	6,490,717	12-03-2002	Pedersen et al		
<i>BT</i>	12.	6,546,539	04-08-2003	Lu et al		

<b>Examiner Signature</b>	<i>M. Het</i>	<b>Date Considered</b>	05/29/04
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				<b>Group Art Unit</b>	2123 <i>2825</i>
				<b>Examiner Name</b>	<i>JAD</i>
<b>Sheet</b>	1	of	1	<b>Attorney Docket Number</b>	SPLX.P0098

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<i>BT</i>	1.	5,521,835		05-28-1996	Trimberger	
	2.	5,610,829		03-11-1997	Trimberger	
	3.	6,035,107		03-07-2000	Kuehlman et al.	
	4.	6,334,205		12-25-2001	Iyer et al.	
	5.	6,470,478	B1	10-22-2002	Bargh et al.	
	6.	6,496,972	B1	12-17-2002	Segal	
	7.	6,523,156	B2	02-18-2003	Cirit	
<i>BT</i>	8.	6,574,779	B2	06-03-2003	Allen et al.	

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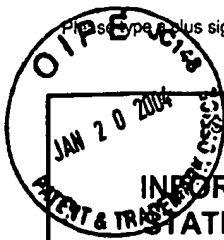
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BS	9.	Yi, J. H. et al., Technology Mapping for Storage Elements Based on BDD matching, Proceedings of the 40 <sup>th</sup> Midwest Symposium on Circuits and Systems, pp. 1099-1102, vol.2, August 1997.			

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				Examiner Name	<i>TAO</i>
Sheet	2	of	2	Attorney Docket Number	SPLX.P009 <b>RECEIVED</b>

U.S. PATENT DOCUMENTS						JAN 22 2004
<i>BA</i>	22.	6,618,835	B1	09-09-2003	Garlapati et al.	Technology Center 2100

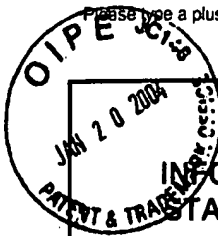
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<i>BA</i>	23.	NN78055443, "Automatic Remap", IBM Technical Disclosure Bulletin, Vol. 20, No. 12, May 1978, pp. 5443-5445 (5 pages).		
<i> </i>	24.	NN9411291, "Design of Portable Library using Parameterized Cells", IBM Technical Disclosure Bulletin, Vol. 37, No. 11, pp. 291-292 (4 pages).		
<i> </i>	25.	Markovic et al., "FPGA to ASIC Conversion Design Methodology with the Support for Fast Retargeting to Different CMOS Implementation Technologies", Proceedings of 2002 22 <sup>nd</sup> International Conference on Microelectronics, Vol. 2, 14 May 2000, pp. 703-706.		
<i> </i>	26.	Ruiz et al., "Design and Prototyping of DSP Custom Circuits Based on a Library of Arithmetic Components", Vol. 1, 9 November 1997, pp. 191-196.		
<i>h</i>	27.	Tamiya, Y., "Delay Estimation for Technology Independent Synthesis", 1997 Proceedings of the ASP-DAC '97, Asia and South Pacific Design Automation Conference, 28 January 1997, pp. 31-36.		

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BT	1.	2002/0157063	A1	10-24-2002	Besson	
	2.	2002/0178432	A1	11-28-2002	Kim et al.	
	3.	2003/0145288	A1	07-31-2003	Wang et al.	
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<b>Substitute for form 1449A/PTO</b>  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)				<b>Application Number</b>	10/061,719
				<b>Filing Date</b>	1/31/02
				<b>First Named Inventor</b>	Steven Teig, et al.
				<b>Group Art Unit</b>	2123 2928
				<b>Examiner Name</b>	TAS
<b>Sheet</b>	1	of	1	<b>Attorney Docket Number</b>	SPLX.P0098

U.S. PATENT DOCUMENTS						
Examiner* Initials	Cite No.	U.S. Patent Document		Date of Publication MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code* (if known)			
RT	1.	6,519,754	B1	02-11-2003	McElvain et al.	

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<b>Title of Invention</b>	Method and apparatus for performing technology mapping																
<p>Application Number: 10/061719 </p> <p>Confirmation Number: 1570</p> <p>First Named Applicant: Steven Teig</p> <p>Attorney Docket Number: SPLX.P0098</p> <p>Art Unit: 2128 <i>2026</i></p> <p>Examiner: <i>Fred O Ferris III</i> <i>AT</i></p> <p>Search string: ( 6216252 ).pn.</p> <p style="text-align: right;"><b>RECEIVED</b> MAR 19 2004 Technology Center 2100</p>																	
<b>US Patent Documents</b>																	
Note: Applicant is not required to submit a paper copy of cited US Patent Documents																	
<table border="1"><thead><tr><th>init</th><th>Cite.No.</th><th>Patent No.</th><th>Date</th><th>Patentee</th><th>Kind</th><th>Class</th><th>Subclass</th></tr></thead><tbody><tr><td><i>B1</i></td><td>1</td><td>6216252</td><td>2001-04-10</td><td>Dangelo et al.</td><td>B1</td><td></td><td></td></tr></tbody></table>		init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass	<i>B1</i>	1	6216252	2001-04-10	Dangelo et al.	B1		
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